ABSTRACT OF THE DISCLOSURE

An SRAM bus architecture includes pass-through interconnect conductors. Each of the pass-through interconnect conductors is connected to routing channels of the general interconnect architecture of the FPGA through an element which includes a pass transistor connected in parallel with s tri-state buffer. The pass transistors and tri-state buffers are controlled by configuration SRAM bits. Some of the pass-through interconnect conductors are connected by programmable elements to the address, data and control signal lines of the SRAM blocks, while other pass through the SRAM blocks with out being further connected to the SRAM bussing architecture.